forming first and second doped regions adjacent to first and second ends of the channel region.

22. The method of claim 21, wherein the first buffer layer is a gate oxide layer, and the second buffer layer is a MgO layer.

23. The method of claim 21, wherein the first buffer layer is an amorphous layer, and the second buffer layer is a highly-oriented layer.

24. The method of claim 23, wherein the second buffer layer has a thickness of no more than 10 nm.

26. The method of claim 21 wherein the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius.

REMARKS

Claims 1-24 and 26 are pending. Claim 25 has been canceled without prejudice pursuant to the restriction requirement. Claims 1, 13, 16, and 18-21 have been amended to correct minor informalities, and to more particularly point out and distinctly claim Applicant's invention. Claim 26 has been added. No new matter has been introduced. Applicant believes the claims comply with 35 U.S.C. § 112.

Claims 1, 3-10, and 13-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by, or in the alternative under 35 U.S.C. § 103(a) as being unpatentable over, Hirai (USP 5,955,755). Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai in view of Yamazaki (USP 6,072,724). Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirai in view of Van Zant and Evetts (USP 5,361,720).

Applicant respectfully submits that amended claim 1 is novel and patentable over Hirai because, for instance, Hirai does not teach or suggest thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer. As described in the specification at page 7, lines 9-20, thermally annealing the buffer layer enhances the alignment of the crystallites of the buffer layer in a highly oriented pattern, which promotes growth of a highly oriented ferroelectric thereon. The annealing step is

particularly useful when working with thin MgO layers since they are more likely to have amorphous or poorly oriented structures as deposited. In one embodiment, the MgO layer is annealed for about 30 minutes in a temperature of 800-1000 degrees Celsius, as recited in dependent claim 13.

The Examiner alleges that Hirai discloses that the buffer layer may be thermally annealed at column 7, lines 38-44. Applicant notes that Hirai merely discloses heating the substrate in the oxidizing atmosphere at a temperature of 650-750 degrees Celsius to form a silicon oxide film under the paraelectric oxide film. Thus, Hirai describes heating the substrate to form the silicon oxide film and is devoid of any teaching or suggestion of thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer. This feature is also absent from the other cited references.

Claims 2-20 depend from claim 1, and are submitted to be patentable as being directed to additional features of the present invention, as well as by being dependent from allowable claim 1. For example, claim 12 recites that the sputtering of the substantially pure magnesium target to form a magnesium oxide buffer layer is maintained at a temperature greater than about 400 degrees Celsius or greater than about 500 degrees Celsius. Claim 13 recites that the buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius for about 30 minutes. These features are completely absent from the references.

Applicant respectfully submits that amended claim 21 is novel and patentable over Hirai because, for instance, Hirai does not teach or suggest thermally annealing the second buffer layer to enhance an alignment of crystallites of the second buffer layer. As described above, Hirai merely discloses heating the substrate in the oxidizing atmosphere at a temperature of 650-750 degrees Celsius to form a silicon oxide film under the paraelectric oxide film. Hirai and the other cited references are devoid of any teaching or suggestion of thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer.

Claims 22-24 and 26 depend from claim 21, and are submitted to be patentable as being directed to additional features of the present invention, as well as by

being dependent from allowable claim 1. For example, claim 23 recites that the first buffer layer is an amorphous layer, and the second buffer layer is a highly-oriented layer. Claim 26 recites that the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius. These features are completely absent from the references.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claim 25 without prejudice; amend claims 1, 13, 16, and 18-21; and add new claim 26.

1. (Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming an oxide layer overlying the substrate;

forming a buffer layer overlying the oxide layer;

thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region.

13. (Amended) The method of claim 11 wherein the buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius for about 30 minutes.

16. (Amended) The method of claim 1 wherein the ferroelectric **[film]** material is substantially free from an amorphous structure.

18. (Amended) The method of claim 1 wherein the buffer layer is a template to provide an oriented growth of the ferroelectric **[film]** material.

19. (Amended) The method of claim 1 wherein the oxide layer is provided by a dry oxidation process comprising an oxygen bearing compound.

20. (Amended) The method of claim 1 wherein the oxide layer passivates the surface of the substrate to protect the channel region.

21. (Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming a first buffer layer overlying the substrate;

forming a second buffer layer overlying the first buffer layer;

thermally annealing the second buffer layer to enhance an alignment of crystallites of the second buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region.

25. CANCELED.

--26. The method of claim 21 wherein the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius.--

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Documents:
1) Information Disclosure Statement Under 37 CFR §1.97 and §1.98
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Applicant: Hong Koo Kim
Application No.: 09/747,779
Filing Date: December 22, 2000
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